sciendo

ISSN 1335-8871

MEASUREMENT SCIENCE REVIEW

Journal homepage: https://content.sciendo.com

Measurement Approach to Evaluation of Ultra-Low-Voltage Amplifier ASICs

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Abstract: This article presents measurement circuits and a test board developed for the experimental evaluation of prototype chip samples of the Fully Differential Difference Amplifier (FDDA). The Device Under Test (DUT) is an ultra low-voltage, high performance integrated FDDA designed and fabricated in 130 nm CMOS technology. The power supply voltage of the FDDA is 400 mV. The measurement circuits were implemented on the test board with the fabricated FDDA chip to evaluate its main parameters and properties. In this work, we focus on evaluation of the following parameters: the input offset voltage, the common-mode rejection ratio, and the power supply rejection ratio. The test board was developed and verified. The test board error was measured to be 38.73 mV. The offset voltage of the FDDA was −0.66 mV. The measured FDDA gain and gain bandwidth were 48 dB and 550 kHz, respectively. In addition to the measurement board, a graphical user interface was also developed to simplify the control of the device under test during measurements.

Keywords: Integrated circuit testing, measurement board, input offset voltage, Common-Mode Rejection Ratio (CMRR), Power Supply Rejection Ratio (PSRR), Fully Differential Difference Amplifier (FDDA).

1. Introduction

Integrated circuits (IC) are ubiquitous and represent a cornerstone of modern electronic systems used in a number of diverse wireless applications. Ultra Large Scale Integration (ULSI) and new manufacturing technologies provide the opportunity to develop (ultra) low-voltage and low-power analog and mixed-signal ICs that can be used, for example, in wearable devices such as cellphones, smartwatches, and smart glasses [1]. However, as the level of integration increases and ICs become more complex, requirements for IC testing also increase [2]. Test and diagnostics are very important and necessary processes of IC development and production flow, and contribute significantly to the final cost of a manufactured chip. The increasing requirements for performance and complexity of ICs make the testing process more difficult and costly.

Nowadays, test engineers need to work more and more closely with design engineers so that they can influence specific details in the IC design to identify potential testability issues and improve test access to specific nodes/circuits in the design. We may assume that with a perfect design and a fair manufacturing process, testing is unnecessary, but the opposite is true. Even a small mistake during the design or a defect in the manufacturing process can have fatal consequences for the entire IC, and therefore, testing should not be underestimated [3]. In order for a design to be easily tested, both controllability and observability must be guaranteed. So let us remember the two well-known features:

- *Controllability* - The ability to control specific parts of a design (specific nodes in the circuit) to set a specific value of a signal. In digital electronics, this would be a logic value (e.i., logic 1 or logic 0); in an analog circuit, it would be a specific voltage or current.
- *Observability* - The ability to observe the response of a circuit to a particular stimulus.

Ensuring controllability and observability should be done as effectively as possible so that additional test hardware does not increase the overall IC price. A traditional approach to IC testing is to finalize the design and leave it to the test engineer to identify, develop and implement a test procedure. Usually, the test is implemented in the form of a software program that controls the external test equipment that is physically connected to a Device Under Test (DUT). If the test engineer realizes at this stage of the test that he or she cannot adequately test the circuit (due to limited controllability/observability), it is usually too late to fix the problem. Modern test approaches involve close collaboration between test engineers and IC designers to assess testability issues early in the design process [4].

This paper presents methods and test circuits for the input offset voltage, Common-Mode Rejection Ratio (CMRR), and Power Supply Rejection Ratio (PSRR) of manufactured Fully Differential Difference Amplifier (FDDA). First, the DUT chip sample is briefly described in Section 2. In Section 3, target parameters for the evaluation are specified. Section 4

DOI: 10.2478/msr-2024-0002

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presents the measurement methods and procedures, the measurement circuits and the developed test board together with the obtained measurement results. In the last section, conclusions are drawn.

2. Device under test (DUT)

An ordinary operational amplifier (op-amp) is an important component of many electronic devices. [5]. The op-amp design process consists of several steps: definition of specifications, selection of component sizes and bias conditions, op-amp stability compensation, simulation, and characterization of key parameters. These include the open-loop gain A_{OL}, PSRR, Common-Mode Range (CMR) at the input, CMRR, the output voltage range, and the power dissipation [6].

Typically, a Differential Difference Amplifier (DDA) is a basic building block of current low-voltage, low-power analog and mixed-signal ICs [7]. Similar to operational amplifiers, the DDAs can be used in various high-performance signal processing circuits such as integrators, filters, multipliers, modulators, etc. [8]. Unlike an ordinary operational amplifier, which has two single-ended inputs, the DDA has four inputs. The circuits with implemented DDA often provide a high input impedance. However, in fully differential signal processing (typically used in low-noise applications), some basic building blocks such as level shifters and voltage followers require a dedicated DDA circuit with differential output, which is called a FDDA.

The general block diagram of an FDDA is shown in Fig. 1. It consists of three main parts:

- input stage,
- current-to-voltage converter, and
- output stage.

The FDDA has two differential inputs that convert two differential voltages into currents. These currents are subtracted from each other and converted back into a differential voltage.

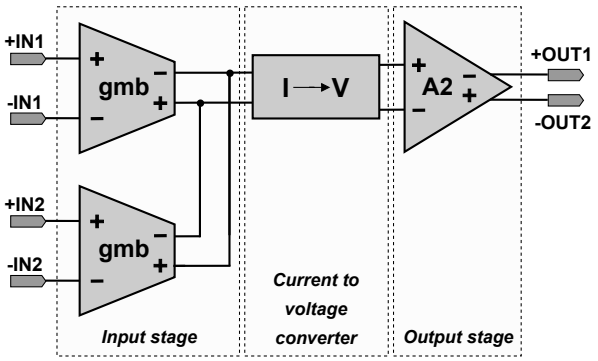

Fig. 1. Block diagram of a FDDA circuit.

The differential output stage amplifies the voltage difference at the output, which can be expressed as follows:

$$V_{OUT} = A[(V_{+IN1} - V_{-IN1}) - (V_{+IN2} - V_{-IN2})] \,, \qquad (1)$$

where A is the total gain, V_{+OUT1} and V_{-OUT2} are the single ended output voltages, $V_{OUT} = V_{+OUT} - V_{-OUT2}$ is the differential output voltage, and $V_{+IN1} - V_{-IN1}$ and $V_{+IN2} - V_{-IN2}$ are the two differential input voltages [9].

The microscope image of the manufactured chip sample with FDDA and other supporting sub-circuits is shown in Fig. 2.

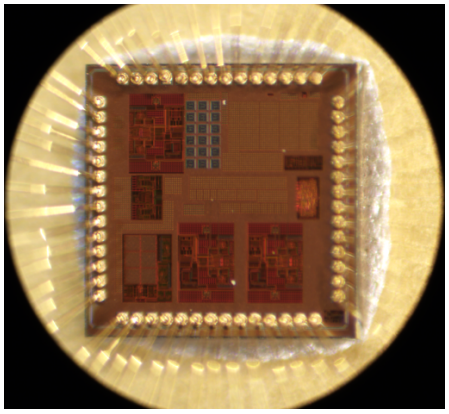

Fig. 2. The photo of the FDDA implemented in a chip.

3. Evaluated parameters and measurement methods

A. *Input offset voltage*

One of the most important parameters of operational amplifiers is the input offset voltage. This random and undesirable parameter is closely related to a possible degradation of other DC or AC amplifier parameters. Therefore, the measurement of this parameter is of great importance [10]. An ideal operational amplifier has zero input offset voltage, zero input current, and an infinite gain [11]. However, all operational amplifiers require a small voltage between their inverting and non-inverting inputs to compensate the mismatch of their input components caused by variations in the manufacturing process. This required voltage is called the input offset voltage and can be modeled by a voltage source (referred to V_{offset}) connected to the input, as shown in Fig. 3. Many techniques are known and used to compensate the input offset voltage. One of the most common techniques is trimming during the production process [12]. Fig. 4 shows a standard circuit for measuring the input offset voltage [13]. The offset voltage can be expressed as shown in (2).

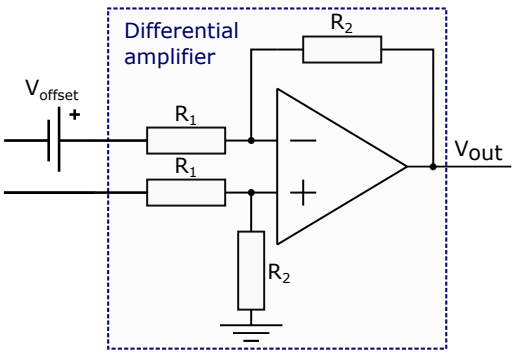

Fig. 3. Modeled input offset voltage in a differential operational amplifier.

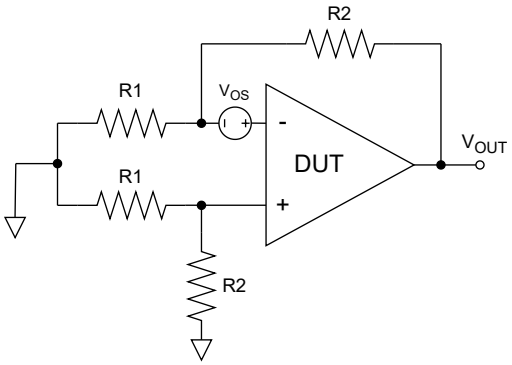

Fig. 4. Standard circuit for measuring input offset voltage.

$$V_{OS} = \frac{V_{OUT}}{1 + \frac{R2}{R1}}, \tag{2}$$

where V_{OS} is the input offset voltage, V_{OUT} is the output voltage and $1 + \frac{R2}{R1}$ is the amplifier gain.

B. Common-Mode Rejection Ratio (CMRR)

An important aspect of the differential amplifier is its ability to suppress a common signal applied to both inputs, which is known as the CMRR parameter. This is one of the most important performance parameters of high-precision operational amplifiers [14]. An ideal operational amplifier does not respond to voltages applied to both inputs. On the other hand, a real operational amplifier may show some response to signals applied to both inputs [15]. The input signal is applied to one input or with opposite polarity to both inputs. These signals are amplified and appear at the output. Unwanted signals that occur with the same polarity (noise) are suppressed by the differential amplifier and only the desired signal appears at the output. This principle of the differential amplifier is shown in Fig. 5.

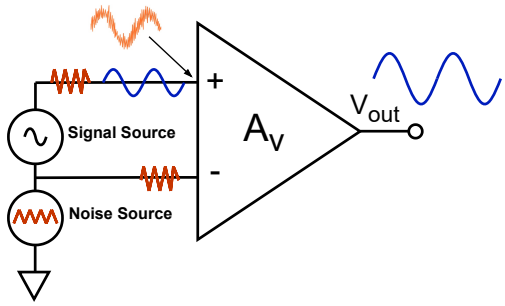

Fig. 5. Description of the CMRR parameter in the differential amplifier.

CMRR parameter is defined as follows:

$$CMRR = \frac{A_{v(d)}}{A_{cm}}, \tag{3}$$

where $A_{v(d)}$ is the ratio of the differential voltage gain and A_{cm} is the common-mode gain. Properly designed differential amplifiers usually have a high differential gain and a low common-mode gain, resulting in a high value of CMRR. The CMRR parameter, expressed in decibels, is as follows:

$$CMRR = 20log\left(\frac{A_{v(d)}}{A_{cm}}\right) \tag{4}$$

Alternatively, CMRR can be expressed as a change in input offset voltage resulting from a unit change in common-mode input voltage. This relation is expressed as follows:

$$CMRR = \frac{\Delta V_{cm}}{\Delta V_{offset}}, \tag{5}$$

where ΔV_{cm} and ΔV_{offset} are the common-mode voltage change and the offset voltage change at the input, respectively.

CMRR can be measured in several ways. The basic measurement circuit is shown in Fig. 6. It consists of a differential amplifier with four precision resistors. A signal is applied to both inputs and the output voltage change is measured. In an amplifier with infinite CMRR, the output would not change at all. To achieve the best result, it is important that the resistors match as closely as possible. A mismatch of 0.1% between two resistor pairs results in a CMRR of only 66 dB (no matter how good the designed amplifier is) [16].

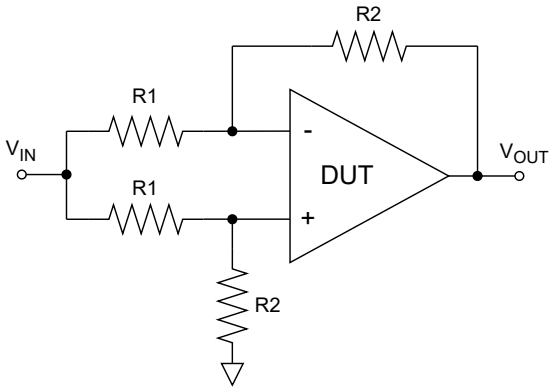

Fig. 6. CMRR measurement circuit.

Then, CMRR can be calculated using the following equation:

$$\Delta V_{OUT} = \frac{\Delta V_{IN}}{CMRR}\left(1 + \frac{R2}{R1}\right), \tag{6}$$

where ΔV_{OUT} is a change in the measured output voltage, ΔV_{IN} is the input voltage change, and $1 + \frac{R2}{R1}$ is the gain of the differential operational amplifier.

C. Power Supply Rejection Ratio (PSRR)

PSRR describes the ability of an amplifier to maintain its output voltage when its DC supply voltage fluctuates. If the supply voltage of an operational amplifier fluctuates, its output voltage should not change. The description of the PSRR parameter is shown in Fig. 7. It shows how fluctuations in the power supply can affect the amplifier output. If a change in the power supply voltage of X volts causes a change in the output voltage as a result of the differential input variation

of Y volts, the PSRR parameter can be defined as the X/Y ratio [17]. PSRR is expressed in decibels as follows:

$$PSRR = -20log\left(\frac{Ripple_{input}}{Ripple_{output}}\right), \tag{7}$$

where $Ripple_{input}$ is the RMS value of the change in V_{IN} at the input, and $Ripple_{output}$ is the RMS value of the voltage change at the output [18]. The measurement setup for the PSRR parameter characterization is the same as that used for CMRR.

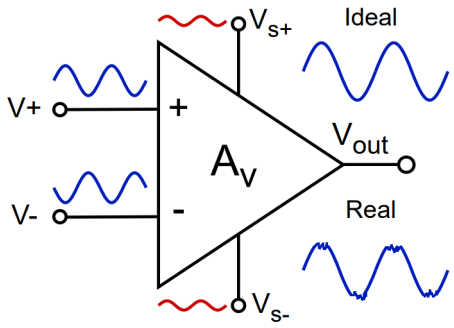

Fig. 7. Influence of power supply variations in the operational amplifier.

4. Proposed Approach to DUT Measurement

The FDDA circuit was designed in the Cadence design environment and the experimental ASIC was prototyped in a general-purpose 130 nm CMOS process. The required measurement circuits were implemented on a chip together with the ASIC system. The measurement circuits are used to verify the correct operation of each block during the evaluation of chip samples on the test board. First, the designed IC was simulated to verify the functionality of the entire system as well as the implemented on-chip measurement circuits and the developed test board, as shown in Fig. 8.

Fig. 8. Developed test board for the evaluation of FDDA samples.

Critical and important nodes of the ASIC were connected to external measurement circuits implemented on the test board. The entire system on the chip and the measurement process are controlled by a developed digital logic unit. The control logic makes the experimental verification much easier to perform and also saves many package pins. Another function of the control logic is to adjust selected parameters of the FDDA. The control logic is governed by a microcontroller implemented on the test board. A Graphical User Interface (GUI) was also developed to simplify experimental verification [19]. The block diagram of the entire measurement setup is shown in Fig. 9. Keysight InfiniVision DSOX2054T 4-channel digital storage oscilloscope with 5 GSPS and 500 MHz of bandwidth, Keysight 33600A Series Waveform Generator, Rohde&Schwarz FSV7 signal analyzer and Rohde&Schwarz HMC 8043 3-channel power supply were used in this setup.

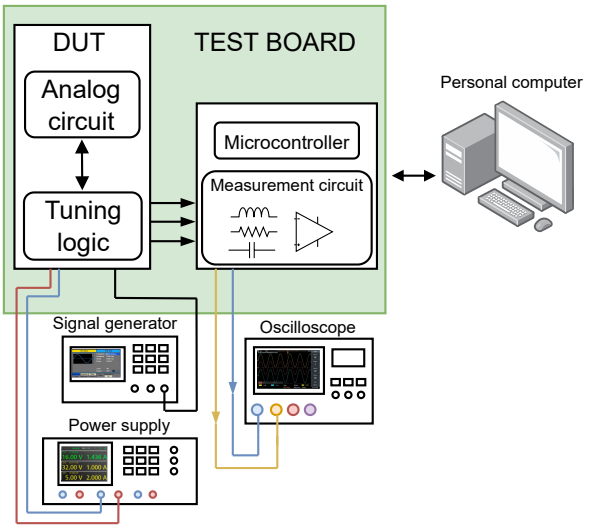

Fig. 9. Block diagram of the measurement setup.

A. FDDA chip sample evaluation

A DC_{LOOP} schematic diagram of the developed FDDA, used for the input offset voltage measurement, is shown in Fig. 10. The DC_{LOOP} gain for IN1+ and IN2- is given by (8) and (9), respectively. The value of DC_{LOOP} gain was set to 200. We have selected MAX4204 device as Buff1 and Buff2, while the MAX4203 device was selected as Buff3 and Buff4. The MAX4204 and MAX4203 are ultra-high-speed, open-loop buffers with high slew rate, high output current, low noise, and excellent capacitive load-driving capability. The MAX4204 device has integrated 50 Ω termination resistors, which are very convenient for driving 50 Ω transmission lines. The MAX4203, on the other hand, has no internal termination resistors [20]. The AMP1 and AMP2 amplifiers were represented by the MAX44250 device, an ultra-precise, low-noise, low-drift amplifier that provides near-zero DC offset and drift through the use of patented auto-correlating zeroing techniques. The best possible circuit components were selected to eliminate their undesirable influence on the measured circuit [21].

$$GAIN(-) = -\frac{Rf_2}{R_4} \tag{8}$$

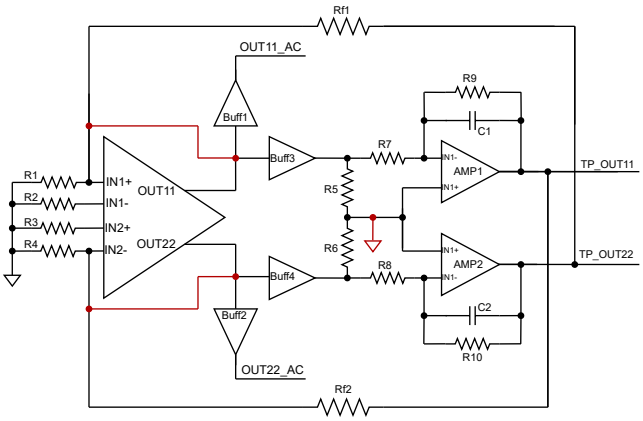

Fig. 10. DC_{LOOP} circuit of FDDA.

$$GAIN(+) = 1 + \frac{Rf_1}{R_1} \tag{9}$$

The DC_{LOOP} configuration with red interconnections (in Fig. 10) was relevant when measuring the test board error ($ERROR_{TB}$), which amounted to 38.73 mV. Since the measurement circuit has a large time constant, the settling time of the measurement was 25 minutes. The input offset voltage of FDDA obtained by the measurement, given by (11), is -0.662 mV. The measurement probes were connected to the nodes labeled TP_OUT11 and TP_OUT22.

$$OFFSET = \frac{DIFF - ERROR_{TB}}{GAIN} \tag{10}$$

$$OFFSET = \frac{(OUT22 - OUT11) - ERROR_{TB}}{GAIN} \tag{11}$$

A schematic diagram of the FDDA circuit for the AC_{LOOP} configuration is shown in Fig. 11. The AC_{LOOP} gain for inputs IN1- and IN2+ is given by (12) and (14), respectively. The AC_{LOOP} configuration gain has been set to 1000. We selected the MAX4204 device as Buff5 and Buff6. The THS4505 device from Texas Instruments was used as a Fully Differential Amplifier (FDA) with a bandwidth of 260 MHz [22].

$$GAIN(-) = -\frac{Rf_3}{R_2} \tag{12}$$

$$GAIN(+) = 1 + \frac{Rf_4}{R_3} \tag{13}$$

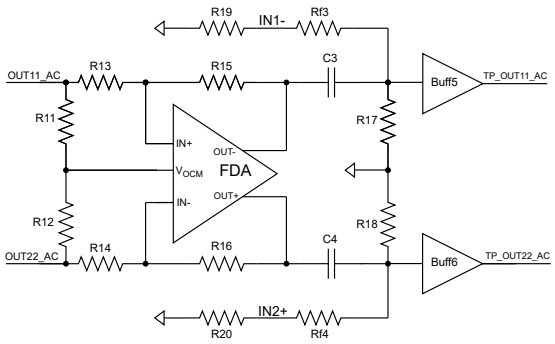

Fig. 11. AC_{LOOP} configuration of FDDA.

The block diagram of the converter from differential input to the single-ended output (D2SE) is shown in Fig. 12. It was designed using the OPA3695 device [23], an operational amplifier with a bandwidth of 900 MHz, which is suitable for instrumentation amplifiers as all three amplifiers are on the same silicon die. The offset matching between the inputs makes this configuration an attractive input stage for this application. The inputs are high impedance, with 1.2 pF capacitance to ground at each input.

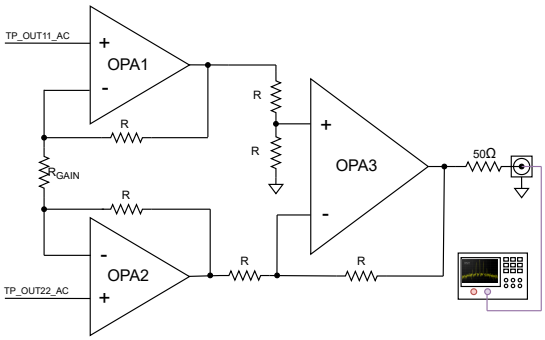

Fig. 12. Differential input to single-ended output converter.

The voltage gain of the instrumentation amplifier is expressed as follows:

$$Av = 1 + \frac{2R}{R_{GAIN}} \tag{14}$$

The gain of the instrumentation amplifier was set to 2 and the converter output was terminated with a 50 Ω resistor. However, the input impedance of a spectrum analyzer was set to 50 Ω so that the measured voltage is in the ratio of 1/1(without gain).

The setup for measuring the frequency response of the DUT is shown in Fig. 13. The DC_{LOOP} gain was set to 200. The signal generator is connected to the IN1- and IN2+ inputs via -60 dB attenuators and resistors R2 and R3. The differential output of the DUT is connected to the oscilloscope via buffers Buff1 and Buff2. The frequency response of the DUT, which was obtained by the measurement of a single package prototype chip at a temperature of 27°C, is shown in Fig. 14. The measured FDDA gain is approximately 48 dB and the gain bandwidth was reported as 550 kHz. The bandwidth value of 2.5 kHz was verified by measurements. The frequency response obtained by simulation is shown in Fig. 15. The DC gain and the gain bandwidth of 43.5 dB and 758.6 kHz, respectively, were achieved.

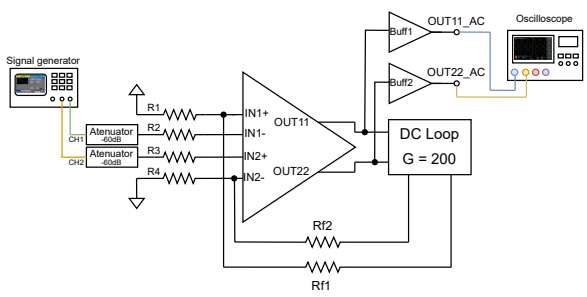

Fig. 13. Measurement setup for frequency response evaluation.

Table 1. Comparison of simulated and measured results of FDDA.

Parameter	Simulated	Measured
DC gain [dB]	43.5	48
GBW [kHz]	758.6	550
CMRR [dB] @1 kHz	91.2	46
PSRR [dB] @1 kHz	73	56
Input offset [mV]	-0.880	-0.662

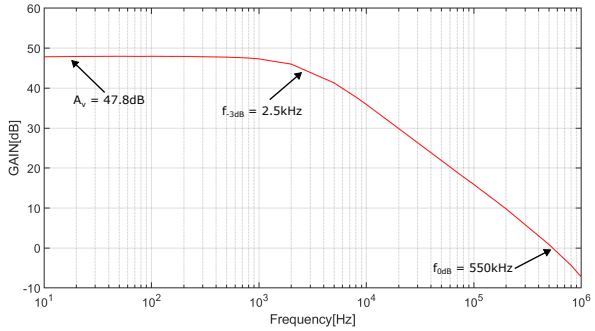

Fig. 14. Frequency response of the FDDA obtained by measurement.

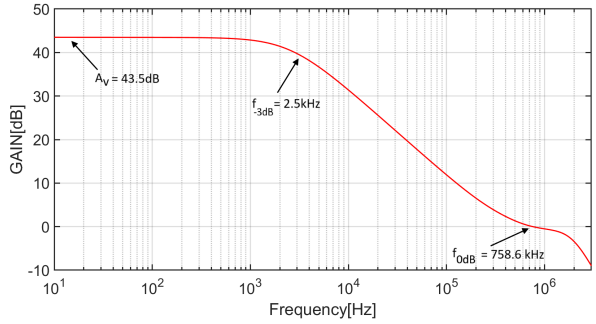

Fig. 15. Frequency response of the FDDA obtained by simulation.

The measurement setup for the evaluation of the CMRR and PSRR parameters is shown in Fig. 16. It is a rather complex circuit, but it does not require precisely matched resistors (like the setup in Fig. 6), which is its main advantage. In this case, the common-mode voltage is changed by switching the power supply voltages. The AC_{LOOP} gain was set to 1000 with resistors Rf3 and Rf4 (see 11), and the DC_{LOOP} gain was set to 200 via resistors Rf2 and Rf1 (see 10). The inputs of FDDA are connected to ground through resistors R1, R2, R3, and R4. The differential outputs of the AC_{LOOP} are fed into the D2SE converter and then connected to the spectrum analyzer via a 50 Ω terminating resistor. Based on the measured voltages, the CMRR and PSRR parameters were calculated using (6) and (7), respectively. The CMRR parameter was measured when the power supply varied in phase (from the positive value to the negative value). For the PSRR parameter measurement, the power supply was varied in the opposite phase. The measured and consequently calculated results are shown in Fig. 17. The PSRR and CMRR parameters obtained by simulation are shown in Fig. 18.

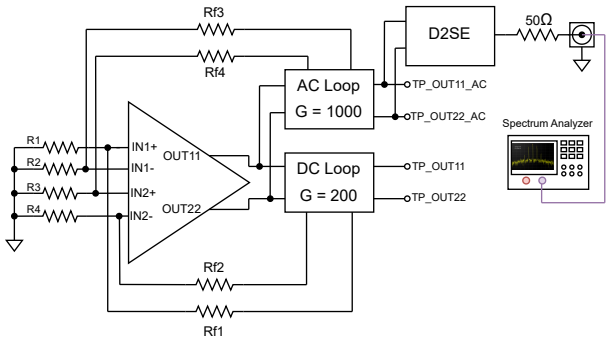

Fig. 16. Measurement setup for CMRR and PSRR evaluation.

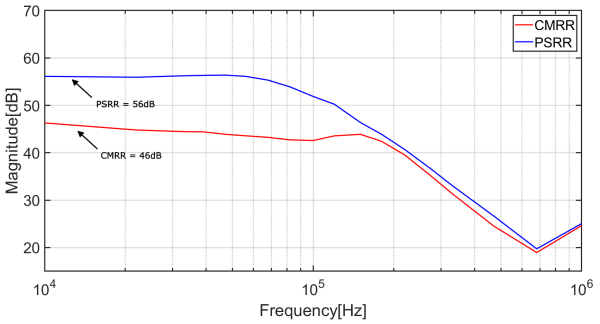

Fig. 17. Measured PSRR and CMRR characteristics.

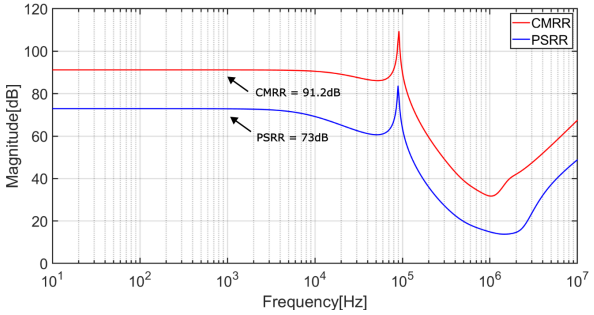

Fig. 18. Simulated PSRR and CMRR characteristics.

B. *Discussion*

The comparison of main parameters of the developed FDDA from simulation and measurement is shown in Table 1. Table 1 shows that the GBW value by measurement decreases from 758.6 kHz to 550 kHz. The correlation of measured values for other parameters such as CMRR and PSRR also decreased. On the other hand, the DC gain and the input offset voltage achieve better results than in the simulation. The deterioration of the measured parameters can be caused by various factors, but most likely variations in the manufacturing process. The measured and simulated results were obtained at a temperature of 27°C. The comparison with other DDA and FDDA amplifiers is shown in Table 2.

Table 2. Comparison with other DDA and FDDA amplifiers.

Parameter	FDDA[24]	DDA[25]	This work
Process [μm]	0.05	0.18	0.13
V_{DD} [V]	0.4	1.8	0.4
I_{DD} [μA]	79.6	10.7	59.8
DC gain [dB]	58.6	131	43.5
GBW [MHz]	2.31	1.1	0.7586
CMRR [dB] @1 kHz	92	-	91.2
PSRR [dB] @1 kHz	-	-	73

5. Conclusion

Measurement circuits for evaluating the main parameters of a high-performance FDDA ASICs are presented. The input offset voltage as well as CMRR and PSRR of FDDA were the target parameters. A measurement board was developed and FDDA chip prototypes were evaluated with this test board. The test board error was measured to be 38.73 mV. The input offset voltage of -0.662 mV was verified by measurements. The measured FDDA gain is approximately 48 dB. The gain bandwidth of 550 kHz and the bandwidth of 2.5 kHz were measured. The total power consumption of the FDDA is 59.8 μA. The evaluation results obtained show that the designed test board and the developed measurement circuits, which were implemented on the test board and also as part of the FDDA chips, can be successfully used for the evaluation of low-voltage, high-performance ASICs.

Acknowledgment

This work was supported in part by the Slovak Research and Development Agency under grant APVV-19-0392 and the by Ministry of Education, Science, Research and Sport of the Slovak Republic under grant VEGA 1/0760/21. This work has also received funding from the Electronic Components and Systems for European Leadership Joint Undertaking under grant agreement No. 876868. This Joint Undertaking is supported by the EU research and innovation program Horizon 2020 and by Germany, the Slovak Republic, the Netherlands, Spain, and Italy.

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Received July 02, 2023
Accepted October 25, 2023